

CS-89-210



July 12, 2001

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#2/705  
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7/24/01

To: Commissioner of Patents and Trademarks  
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572  
20 McIntosh Drive  
Poughkeepsie, N.Y. 12603

Subject:

Serial No. 09/839,963 04/23/01

Sangki Hong, Subhash Gupta,  
Paul Kwok Keung Ho

A METHOD TO FORM SELF-ALIGNED  
ANTI-VIA INTERCONNECTS

Grp. Art Unit: 2812

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation  
In An Application.

The following Patents and/or Publications are submitted to  
comply with the duty of disclosure under CFR 1.97-1.99 and  
37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 5,512,514 to Lee, "Self-Aligned Via and  
Contact Interconnect Manufacturing Method", teaches a method to  
form an integral via and contact interconnect.

U.S. Patent 5,693,568 to Liu et al., "Reverse Damascene  
Via Structures", discloses a method to form reverse damascene  
interconnects.

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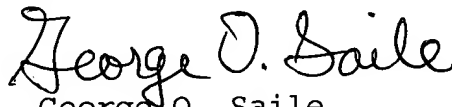
U.S. Patent 4,917,759 to Fisher et al., "Method for Forming Self-Aligned Vias in Multi-Level Metal Integrated Circuits", teaches a method to form self-aligned vias.

U.S. Patent 5,861,673 to Yoo et al., "Method for Forming Vias in Multi-Level Integrated Circuits, for Use with Multi-Level Metallizations", teaches a method to extend the surface area of a metal region wherein a via contact is planned.

U.S. Patent 5,846,876 to Bandyopadhyay et al., "Integrated Circuit Which Uses a Damascene Process for Producing Staggered Interconnect Lines", discloses a method to form damascene interconnects with staggered levels.

U.S. Patent 5,691,238 to Avanzino et al., "Subtractive Dual Damascene", teaches a reverse damascene method.

Sincerely,

A handwritten signature in cursive script that reads "George O. Saile". The signature is written in dark ink and is positioned above the printed name and registration number.

George O. Saile,  
Reg. No. 19572